

FIG. 1

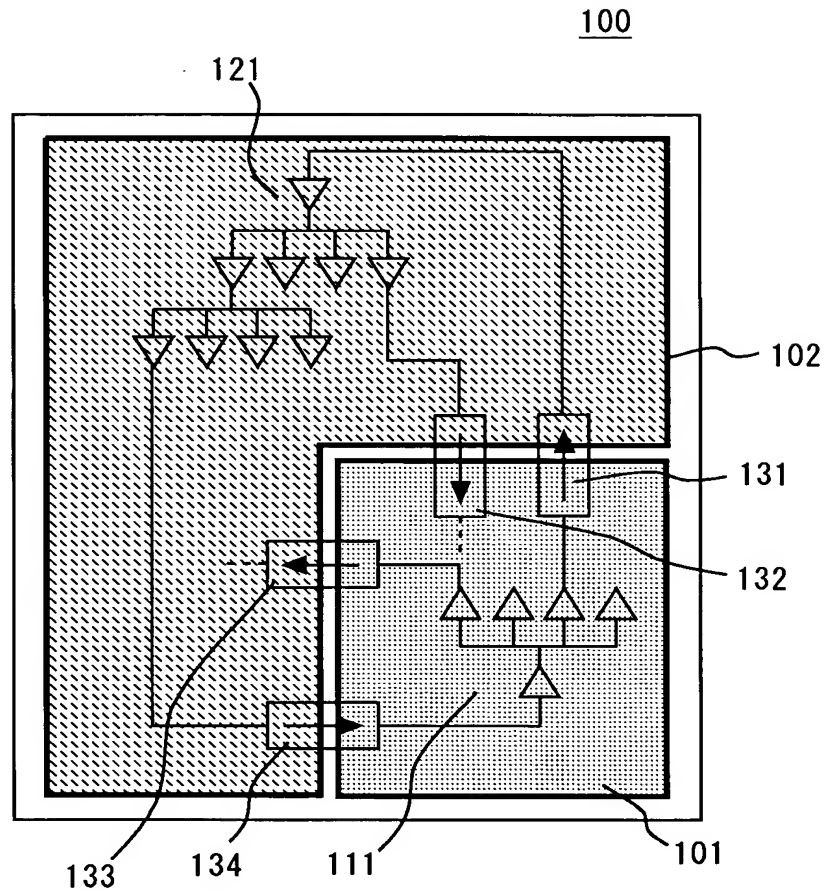


FIG. 2A

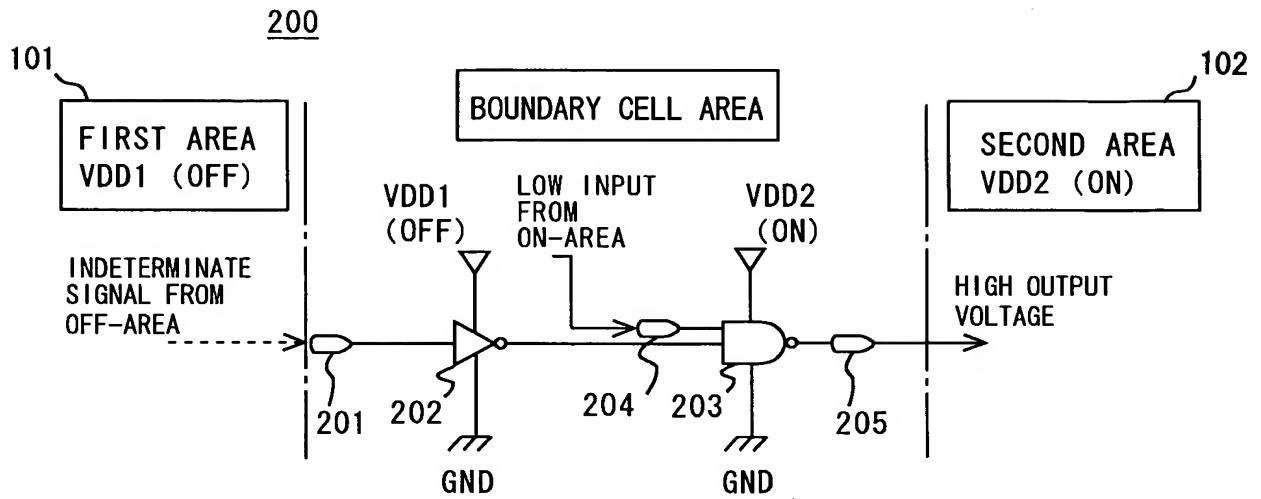


FIG. 2B

INPUT	ENABLE	OUTPUT
0	1	0
1	1	1
X	1	X
X	0	1
X	X	X

FIG. 3A

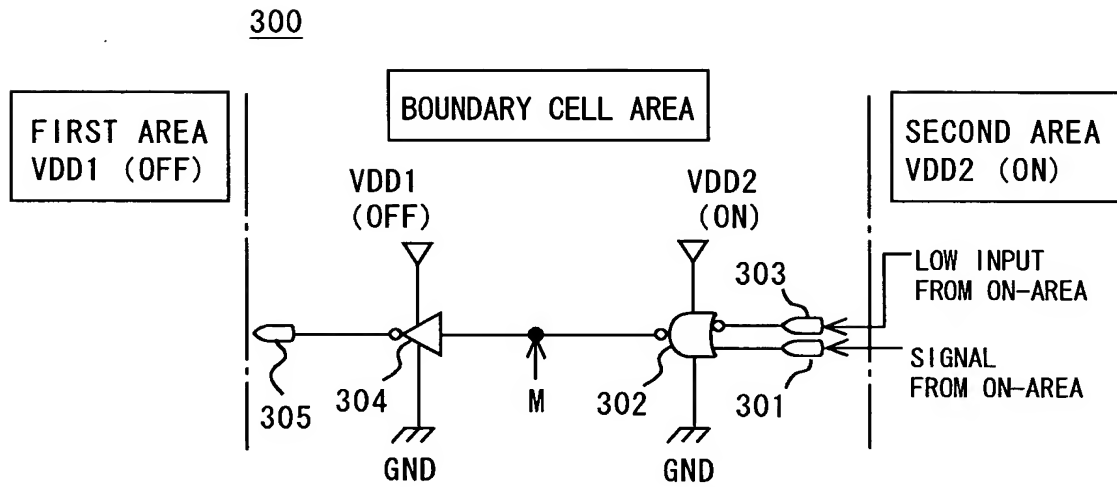


FIG. 3B

INPUT	ENABLE	M	OUTPUT
0	1	1	0
1	1	0	1
X	1	X	X
X	0	0	1
X	X	X	X

FIG. 4A

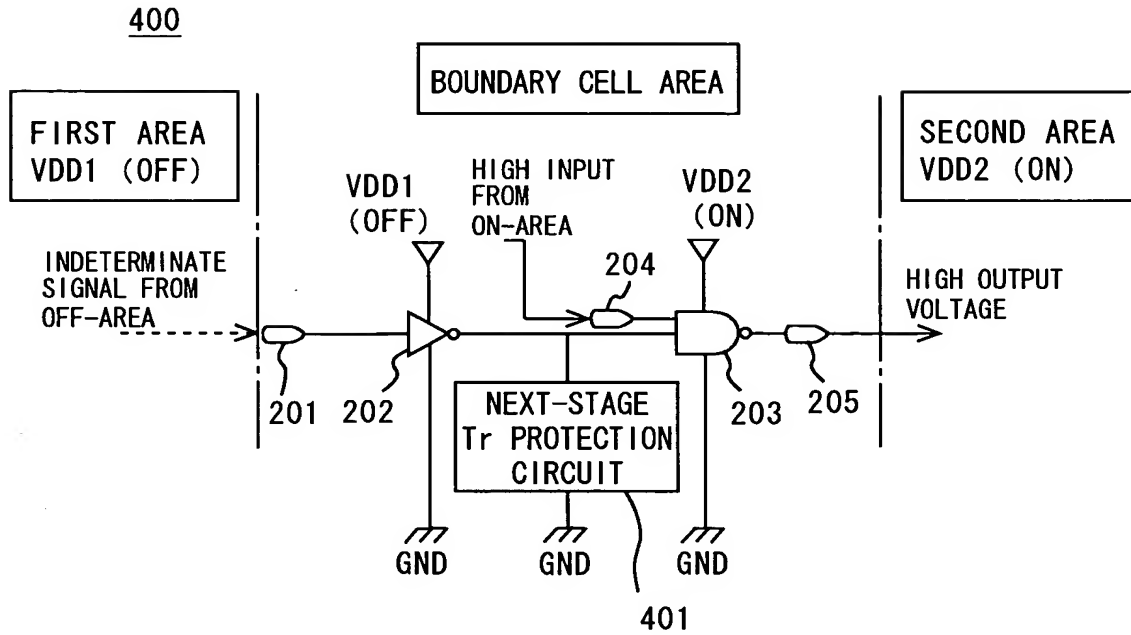


FIG. 4B

INPUT	ENABLE	OUTPUT
0	1	0
1	1	1
X	1	X
X	0	1
X	X	X

FIG. 5A

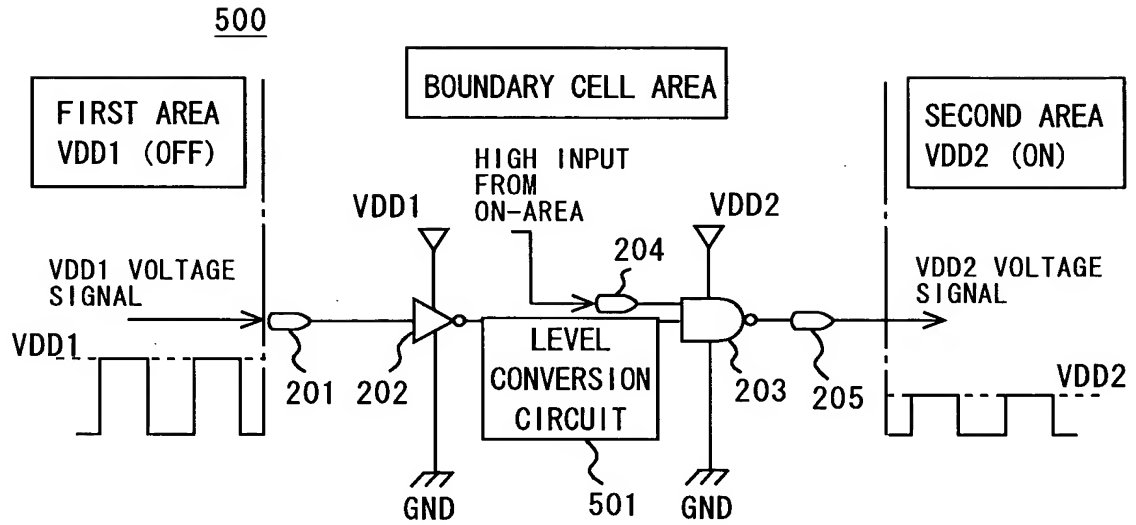


FIG. 5B

INPUT	ENABLE	OUTPUT
0	1	0
1	1	1
X	1	X
X	0	1
X	X	X

FIG. 6

600

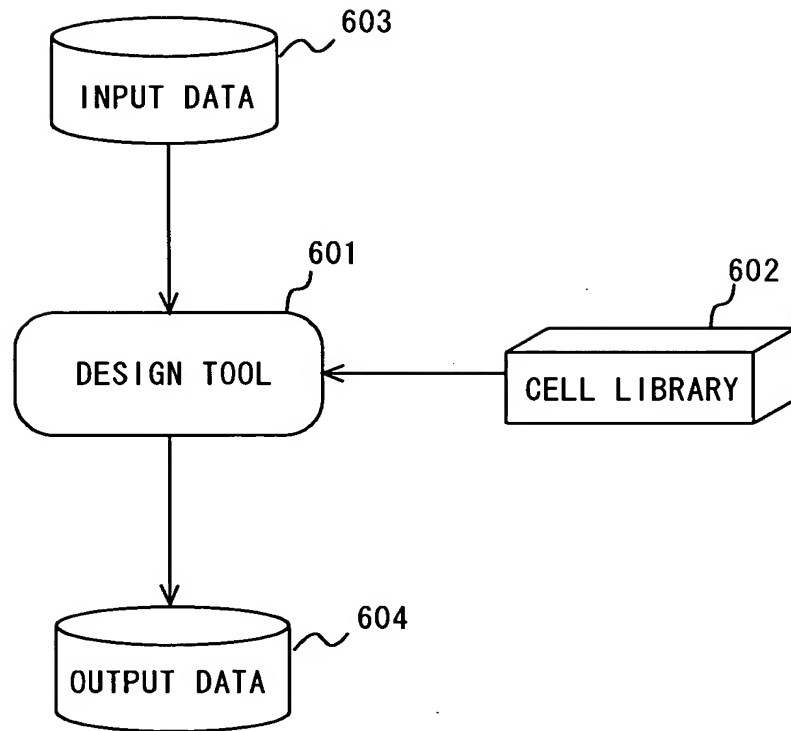


FIG. 7

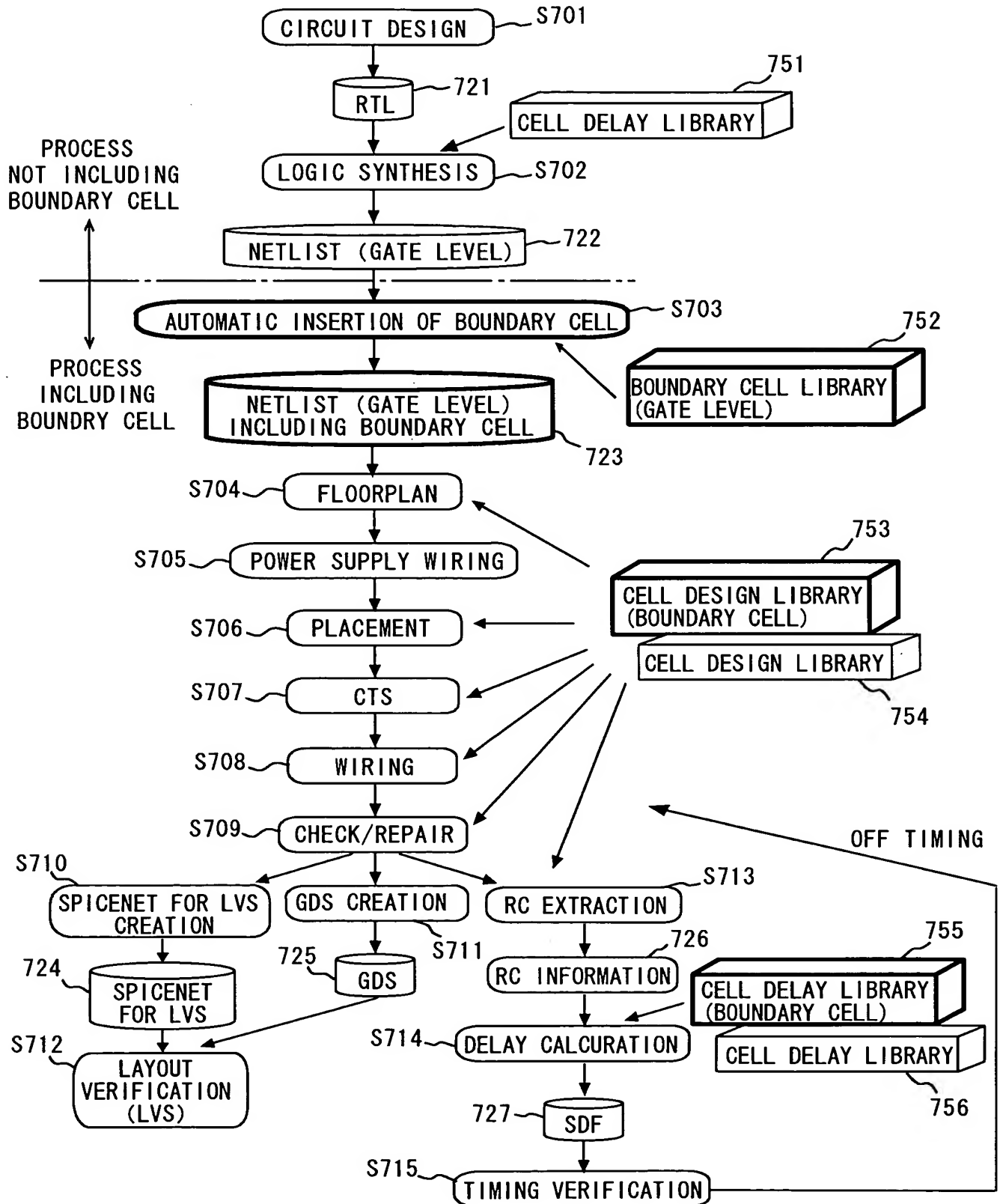


FIG. 8

